

FIG. 1

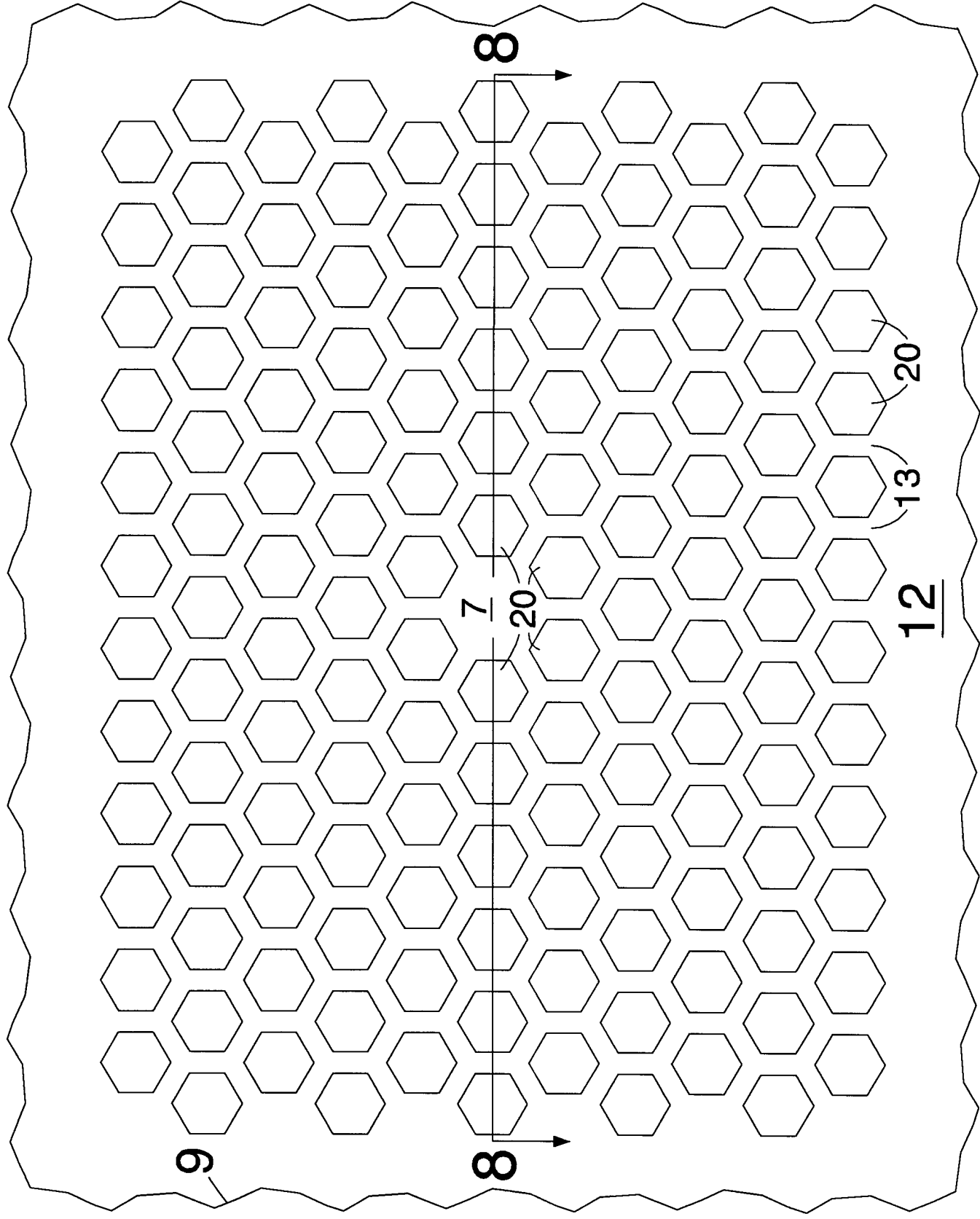


FIG. 2

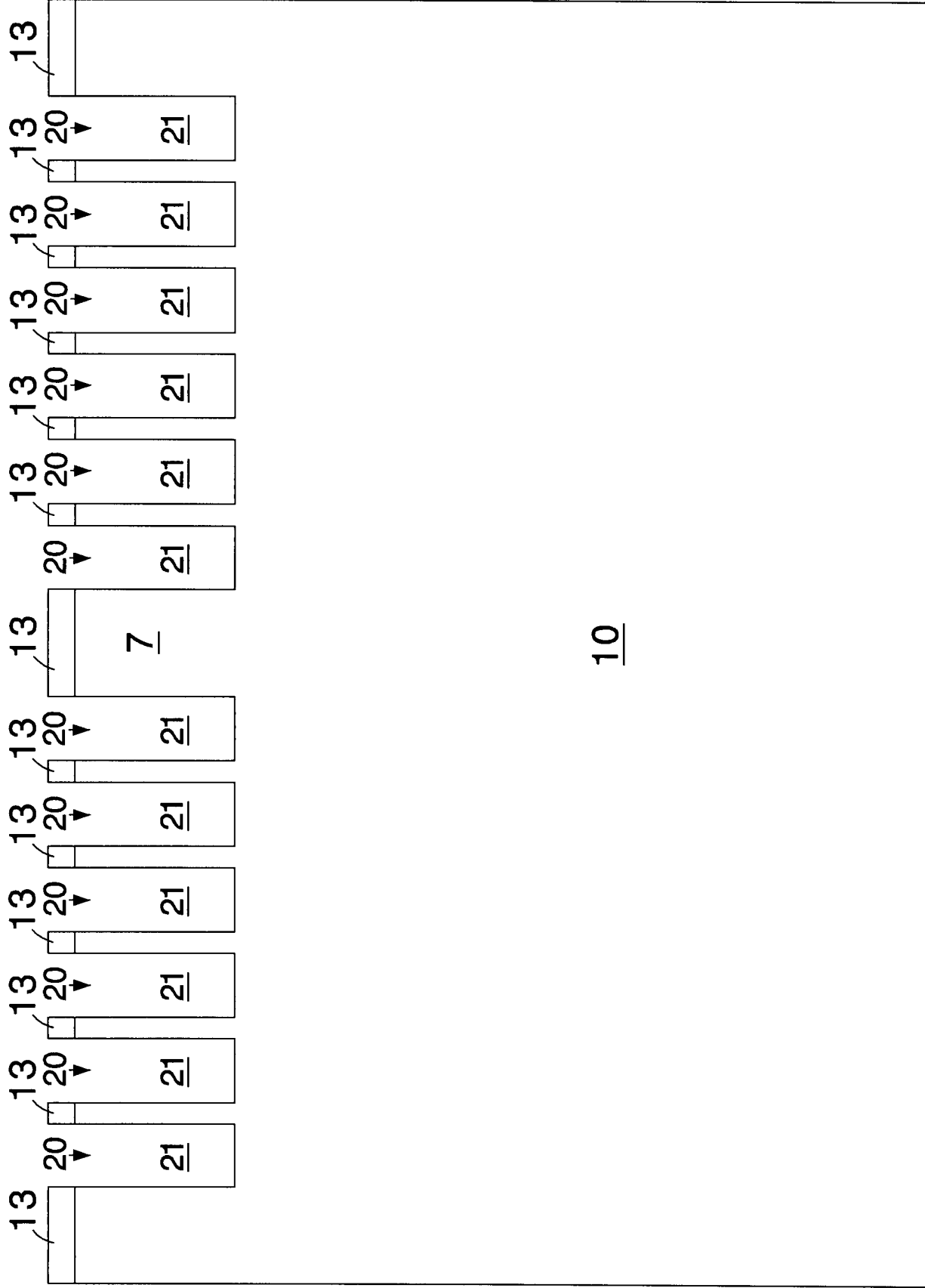
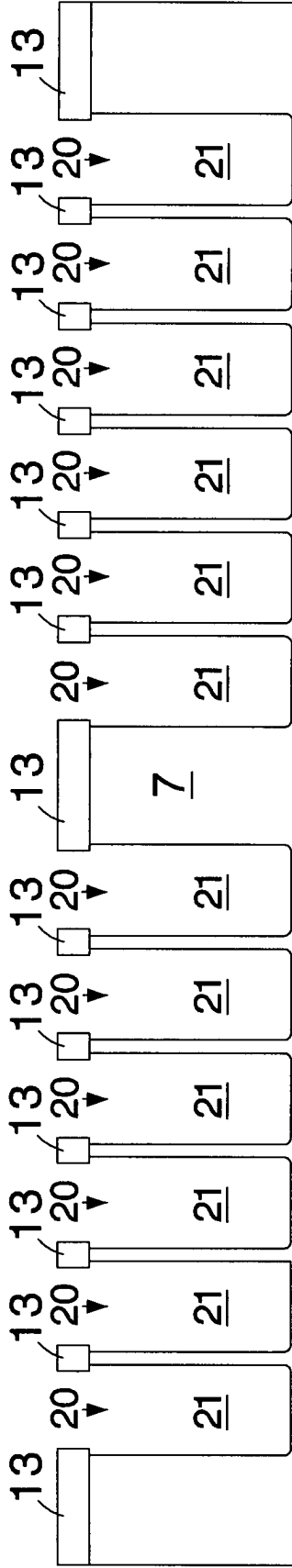
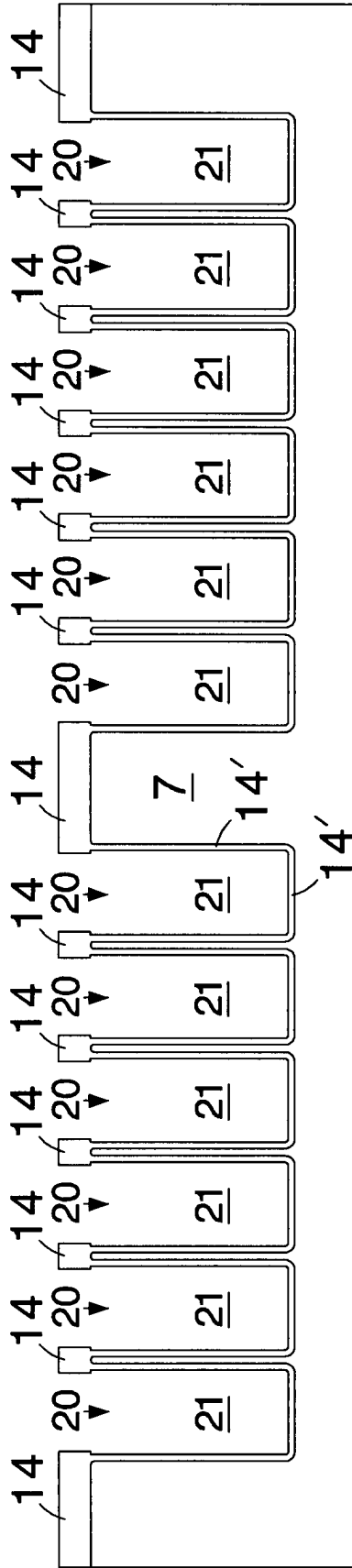


FIG. 3



10

FIG. 4



10

FIG. 5

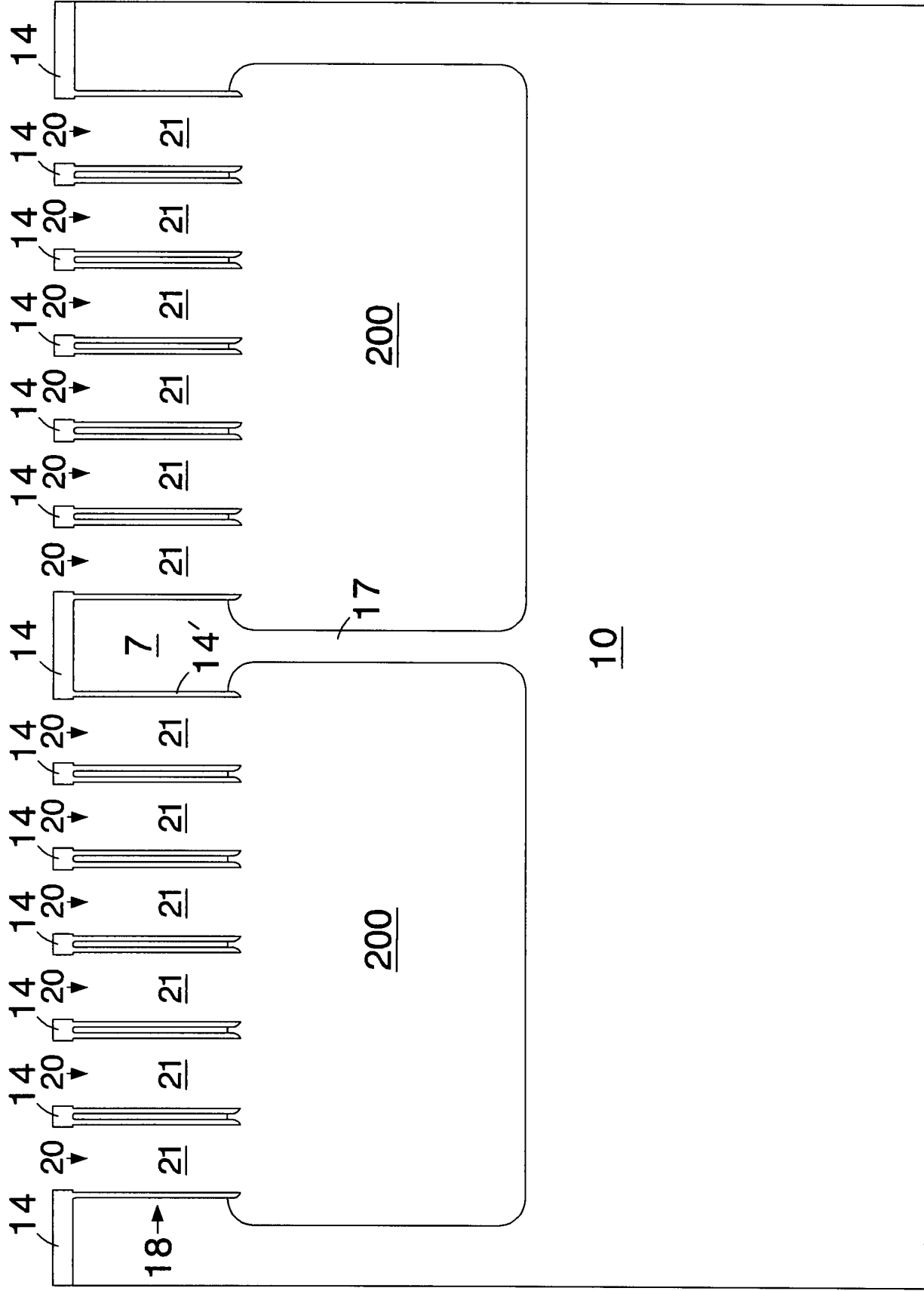


FIG. 6

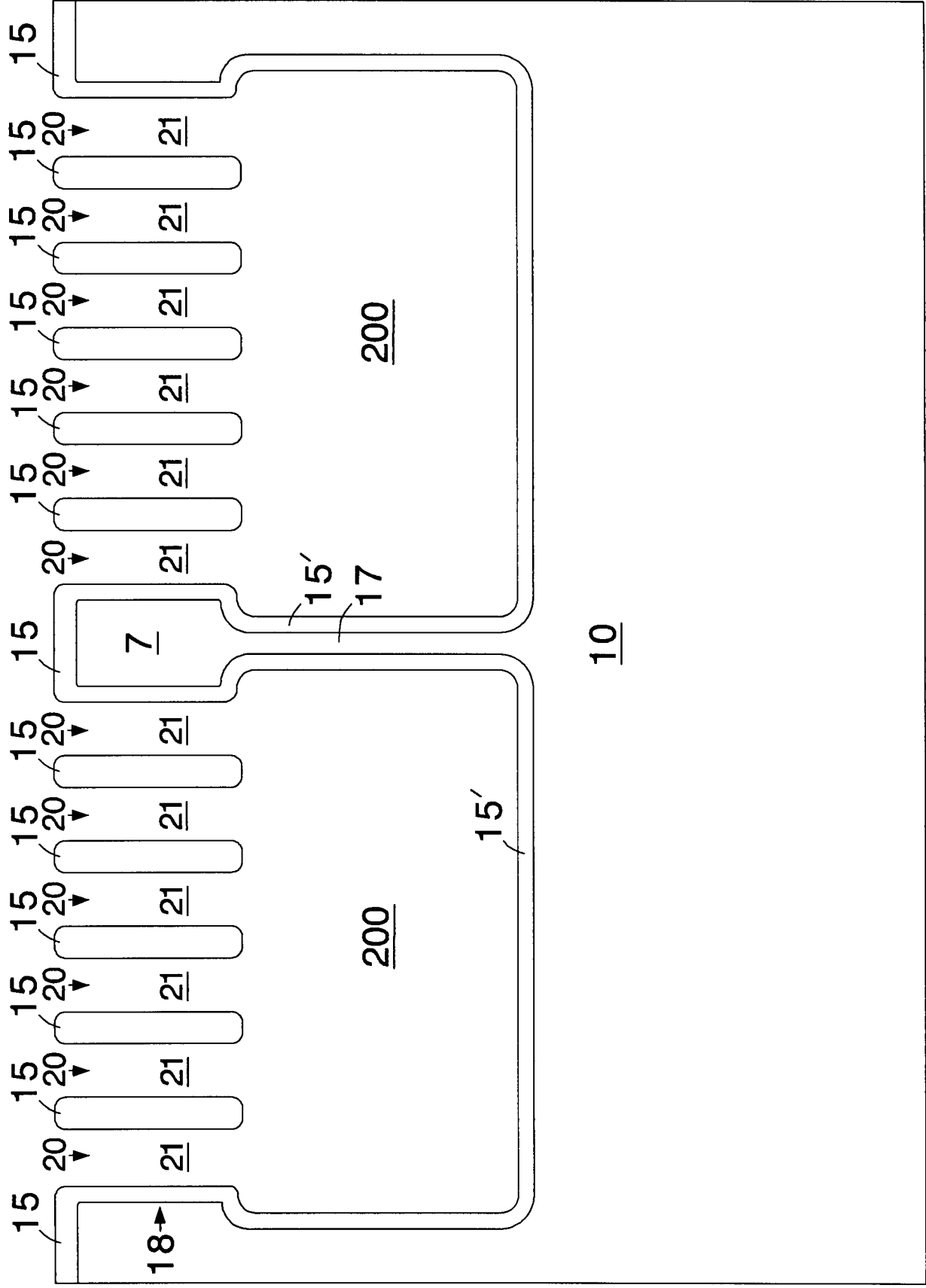


FIG. 7

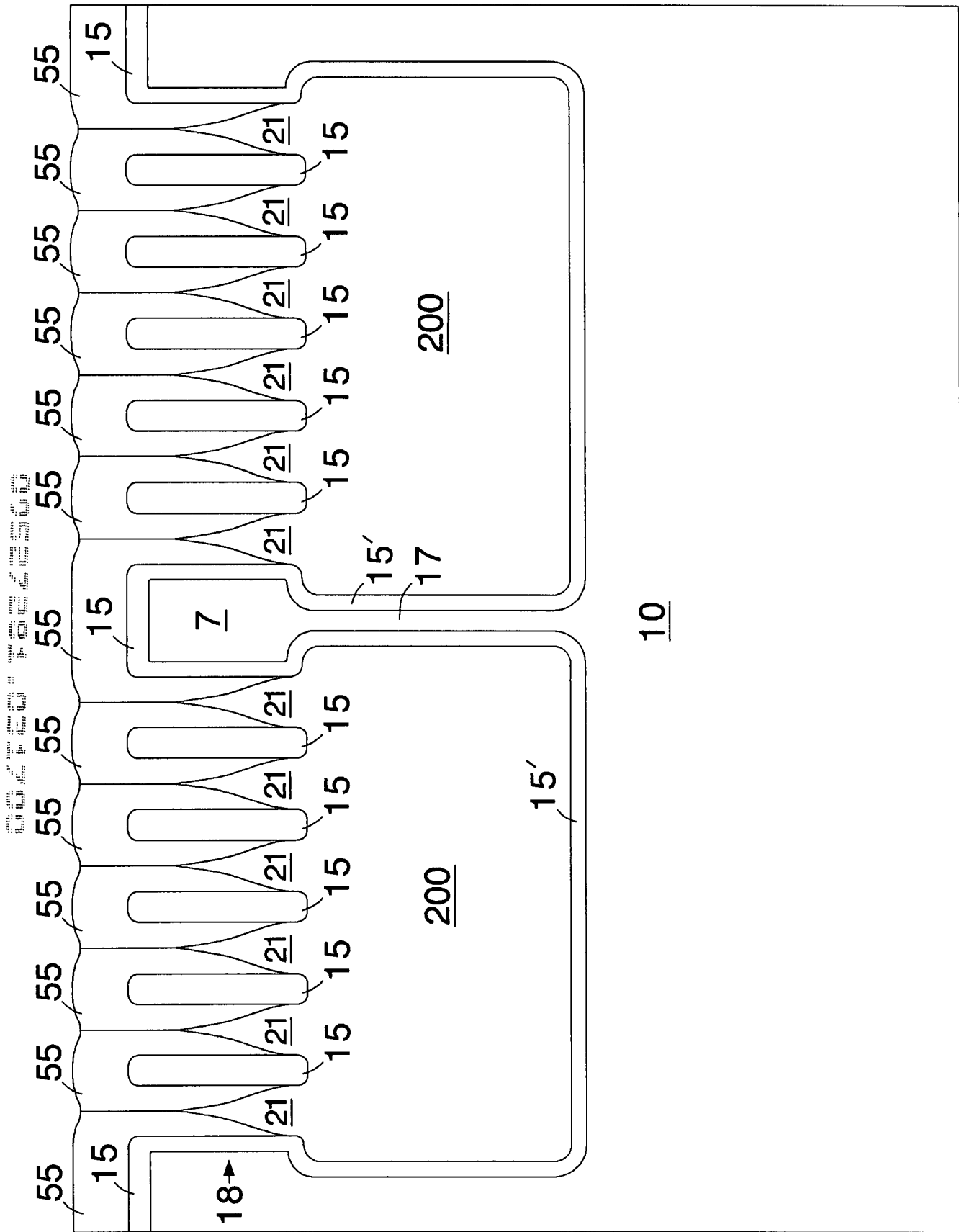


FIG. 8

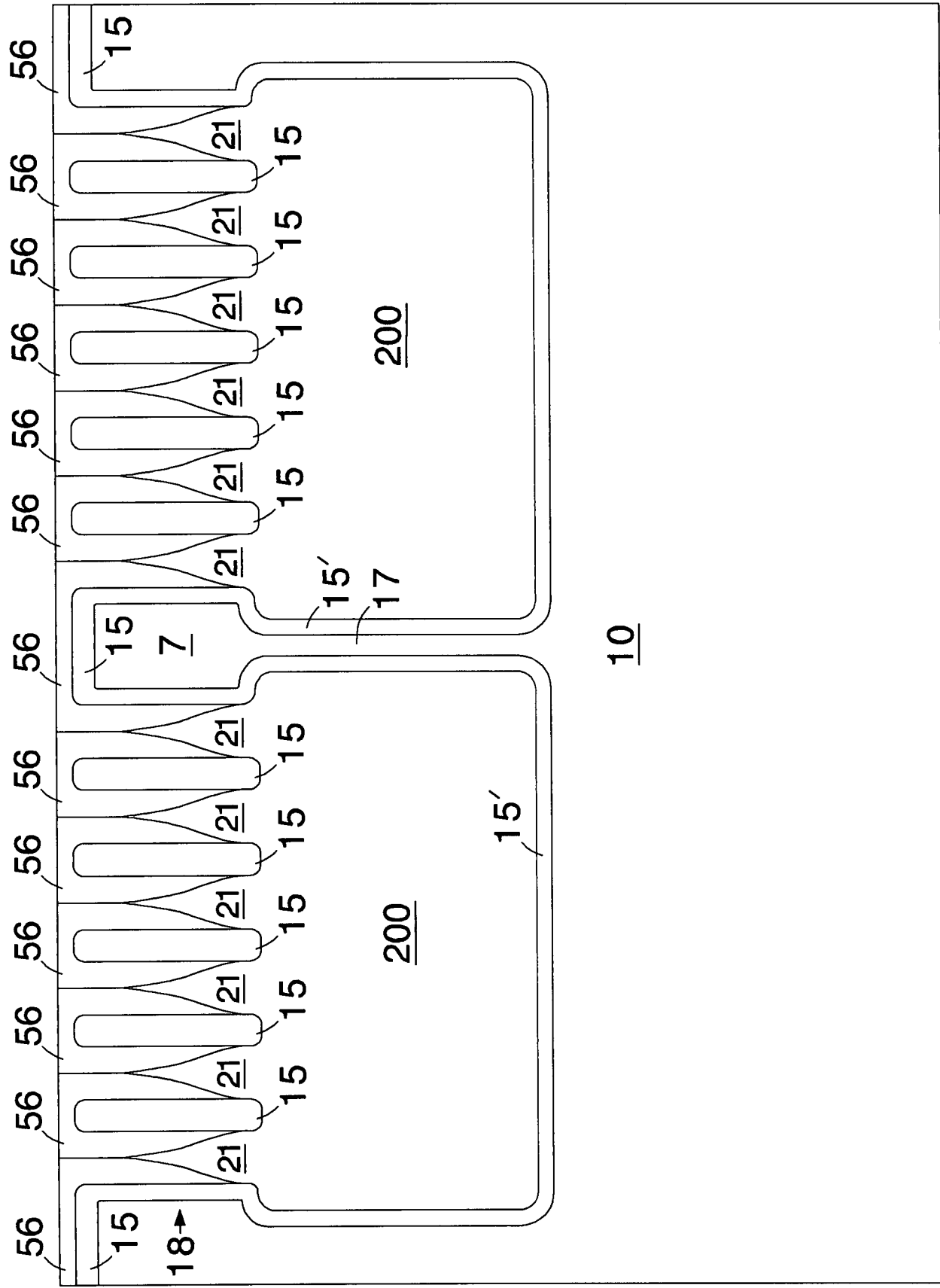


FIG. 9

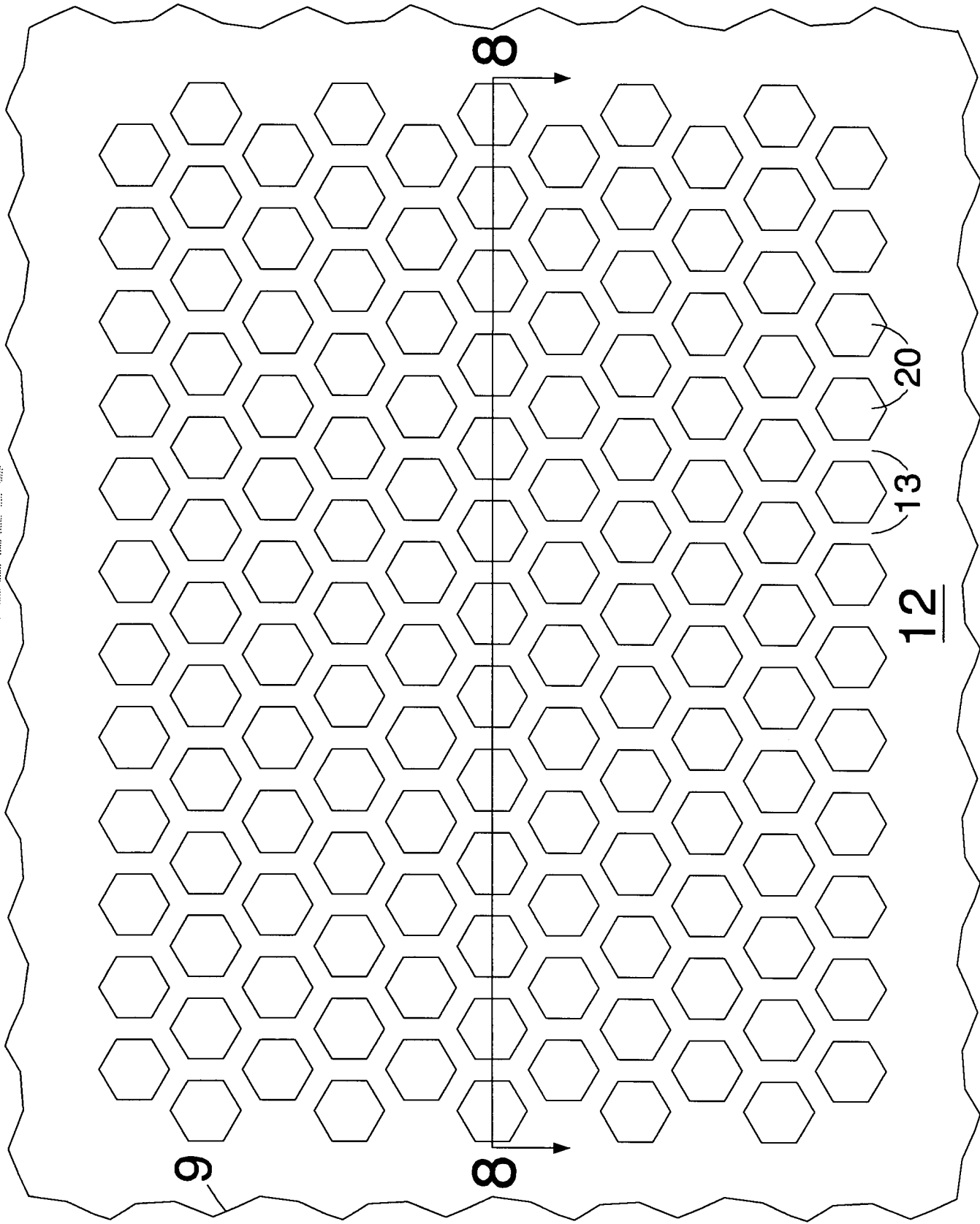


FIG. 10

FIG. 11 is a schematic diagram of a device 10, showing a series of vertical bars 15, each having a top edge 56 and a bottom edge 55. The bars are connected by a horizontal line 21. The device 10 is shown in a perspective view, with the bars 15 and the horizontal line 21 being the main components. The top edge 56 and bottom edge 55 are indicated by dashed lines. The horizontal line 21 is shown as a solid line. The device 10 is shown in a perspective view, with the bars 15 and the horizontal line 21 being the main components. The top edge 56 and bottom edge 55 are indicated by dashed lines. The horizontal line 21 is shown as a solid line.

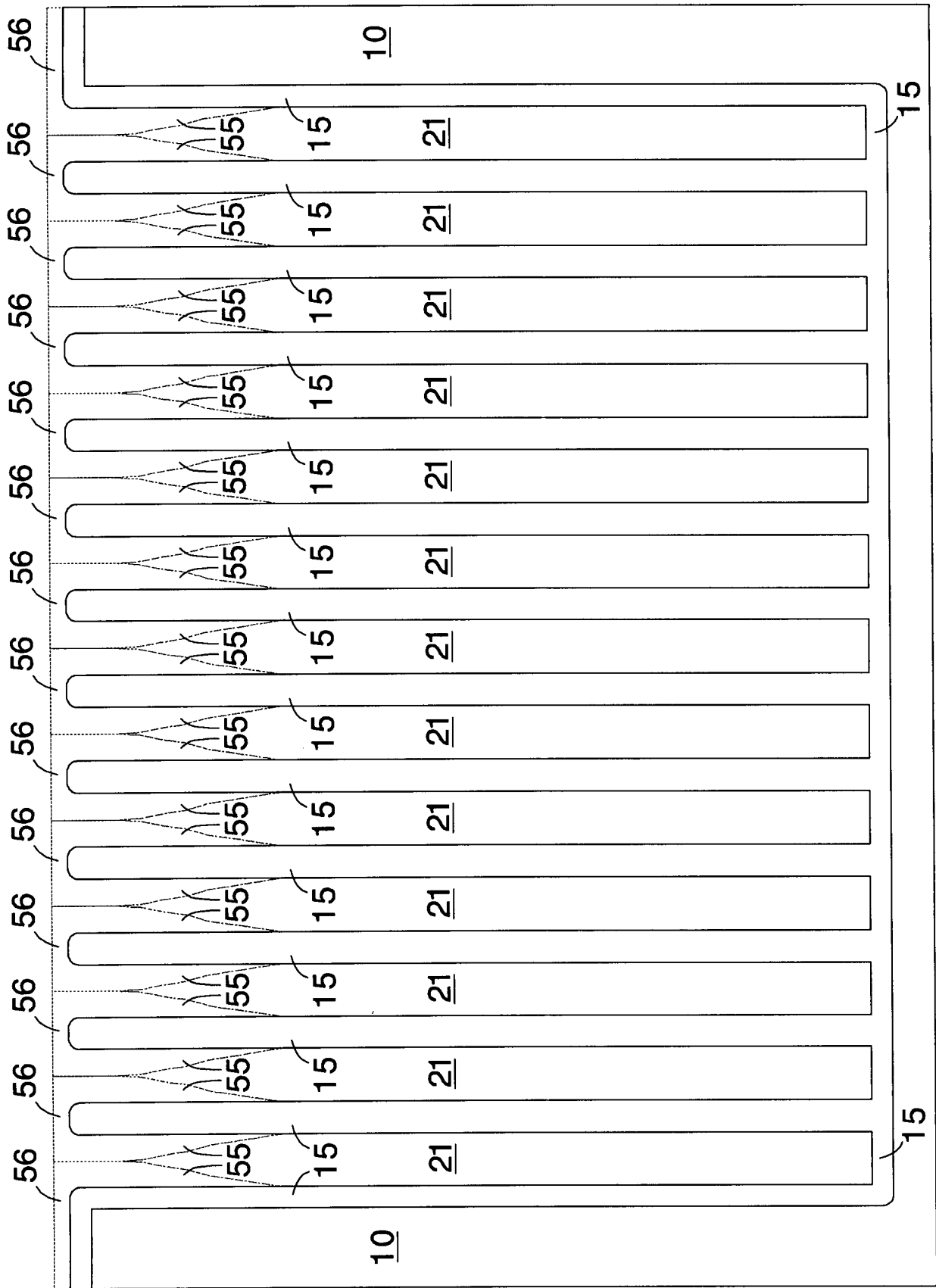


FIG. 11

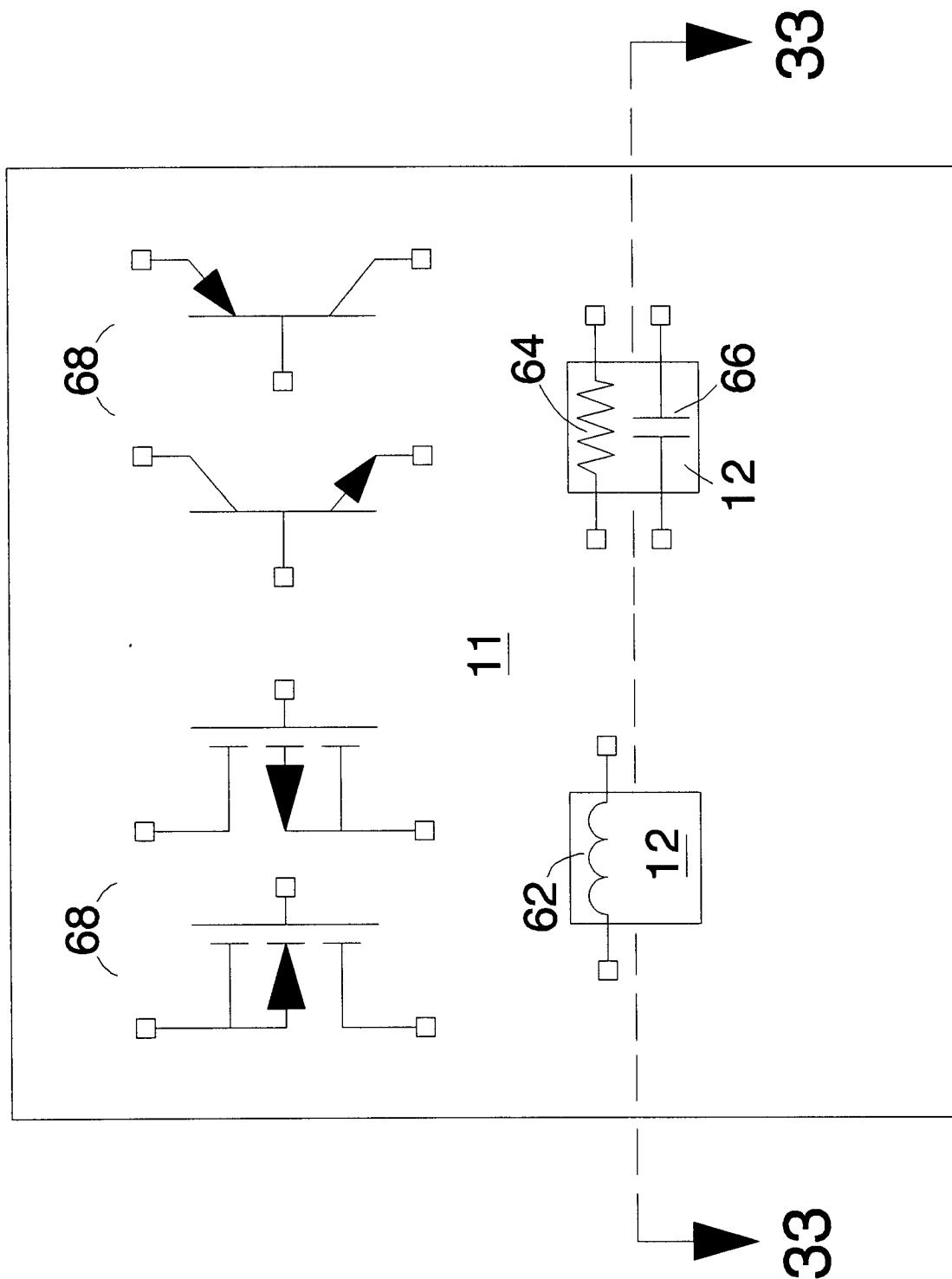


FIG. 12

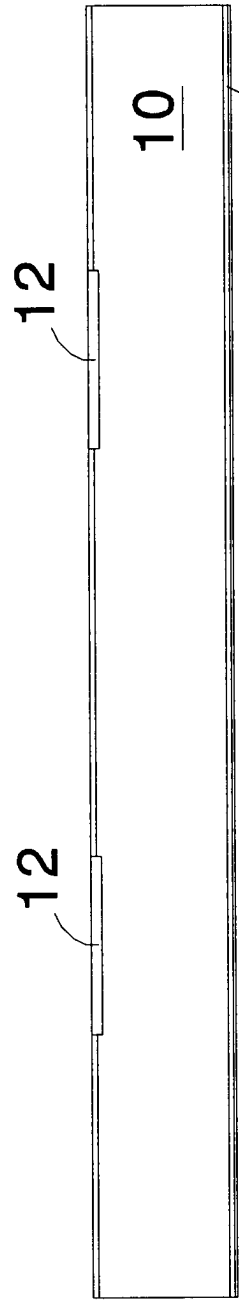


FIG. 13 A

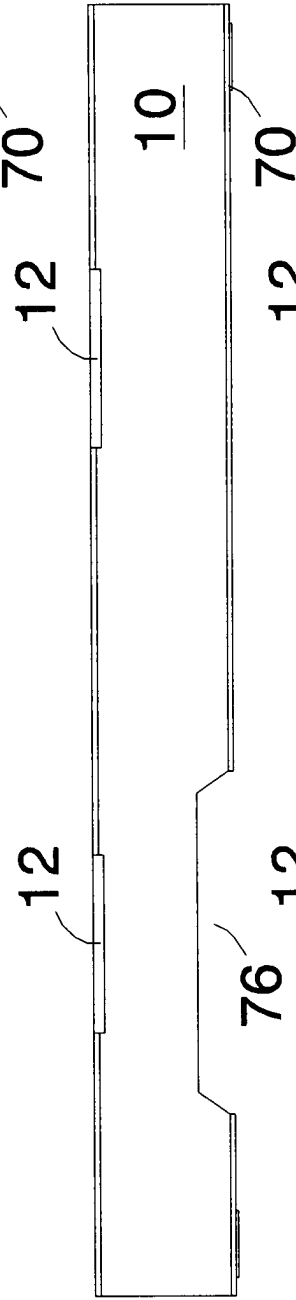


FIG. 13 B

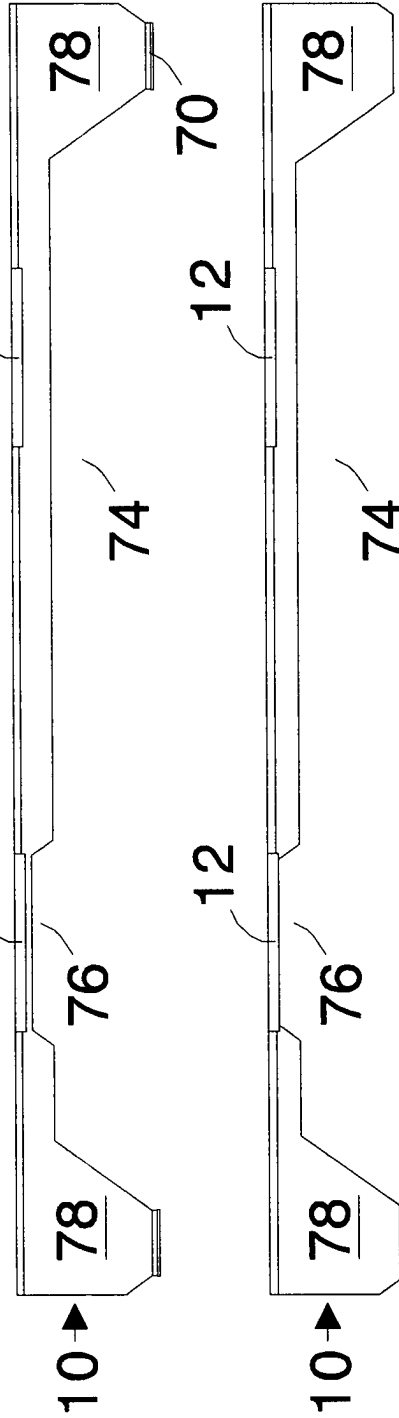


FIG. 13 C

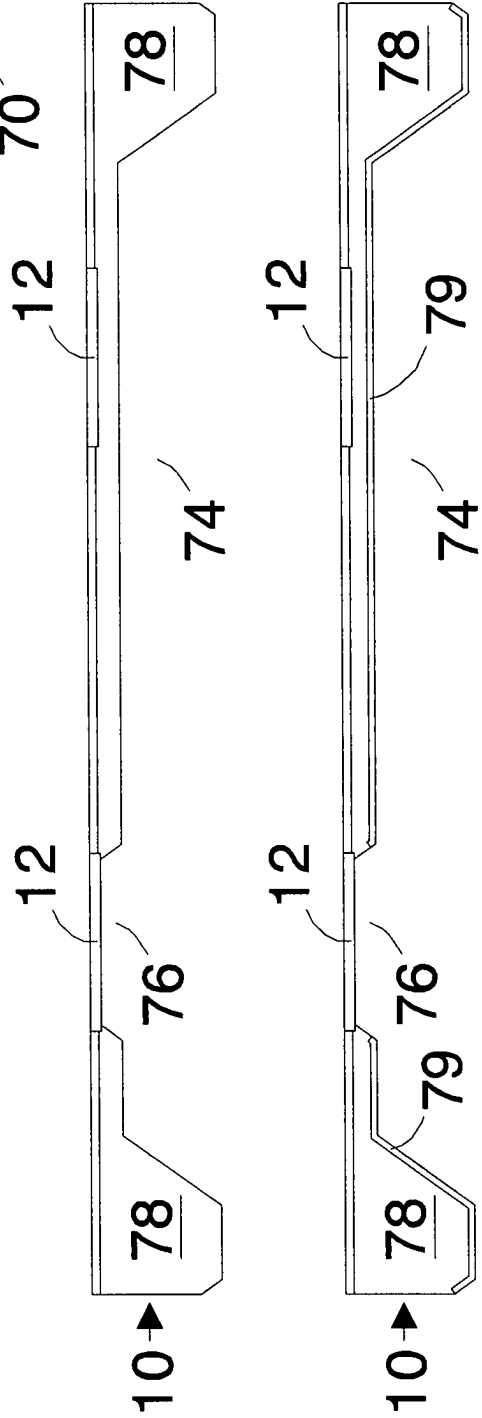


FIG. 13 D

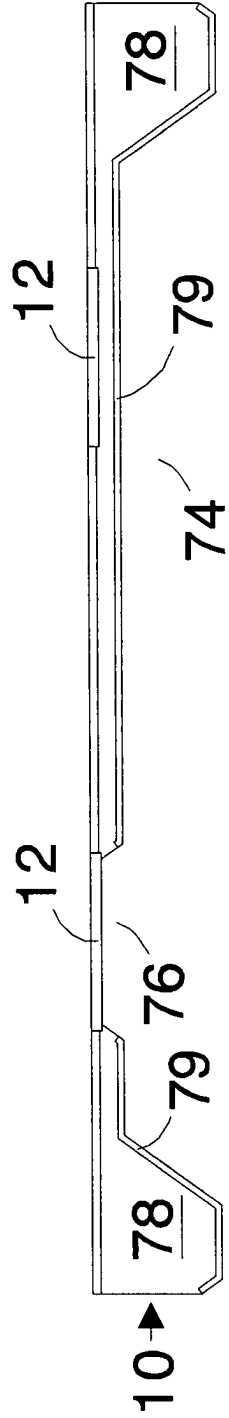


FIG. 13 E

FIG. 14 is a schematic diagram of a circuit 35, which includes a first section 80 and a second section 82. The first section 80 includes a first input 12, a first output 62, a first input 64, a first output 66, a first input 68, a first output 86, a first input 88, and a first output 90. The second section 82 includes a first input 12, a first output 62, a first input 64, a first output 66, a first input 68, a first output 86, a first input 88, and a first output 90.

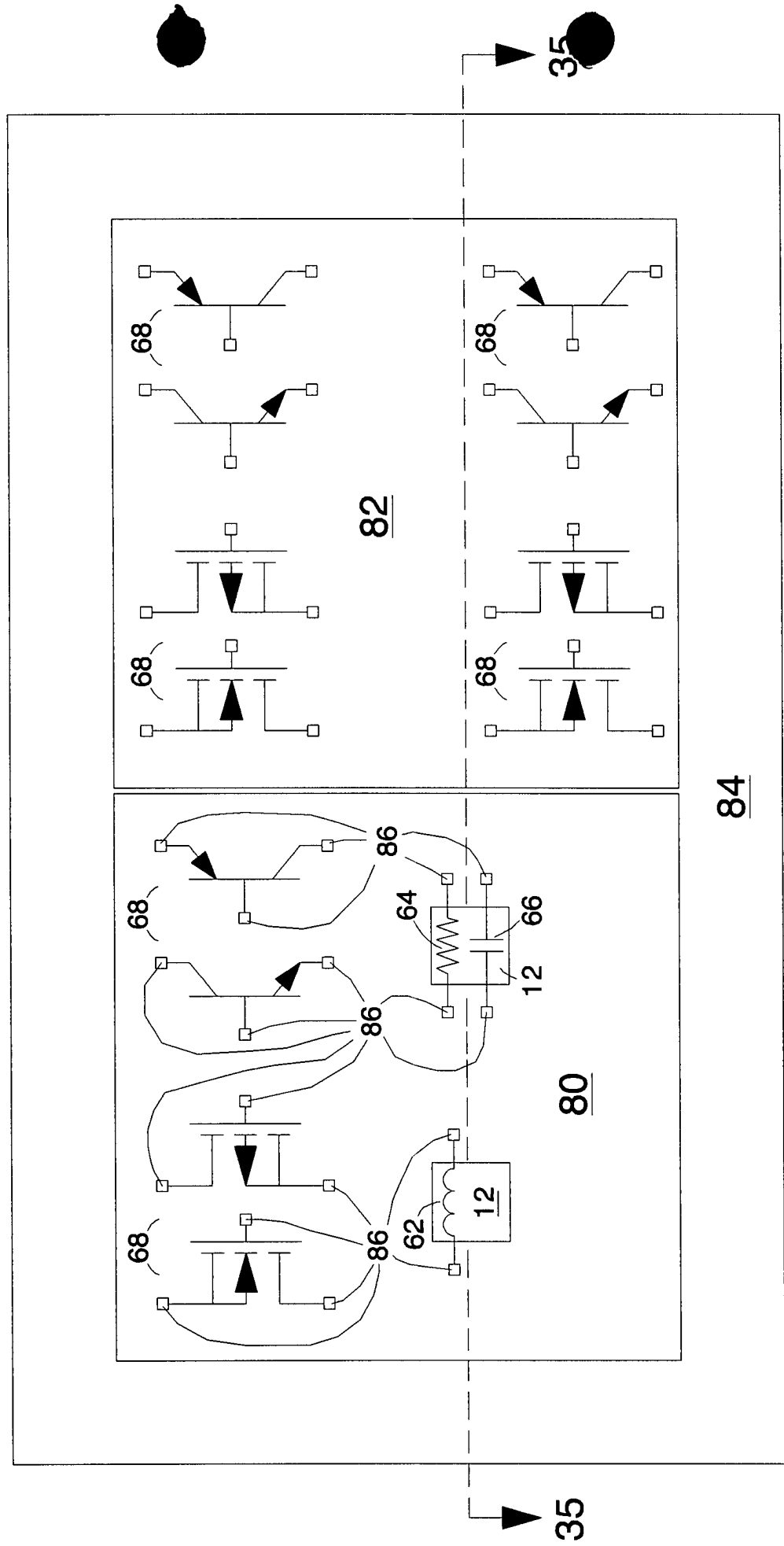
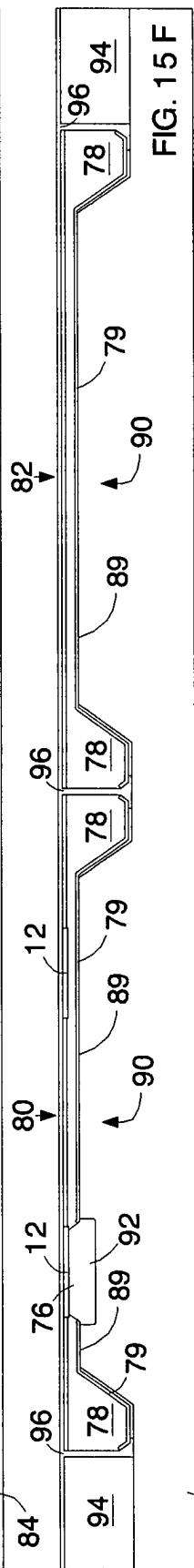
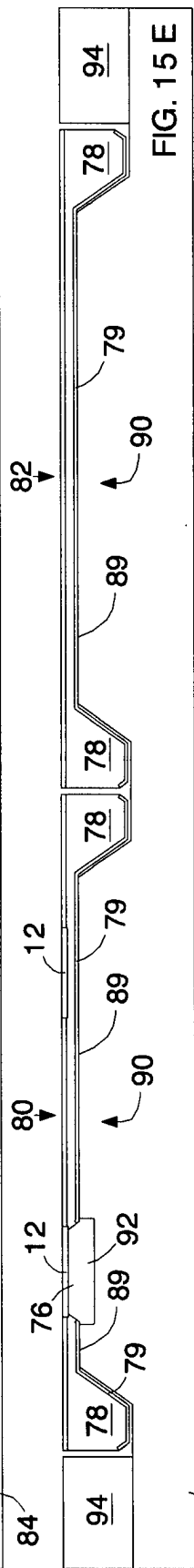
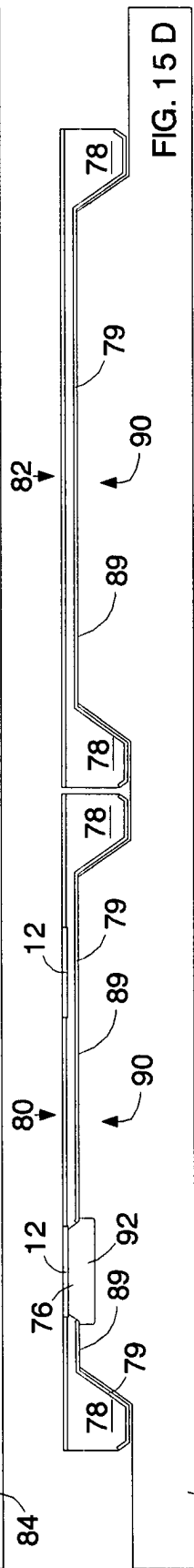
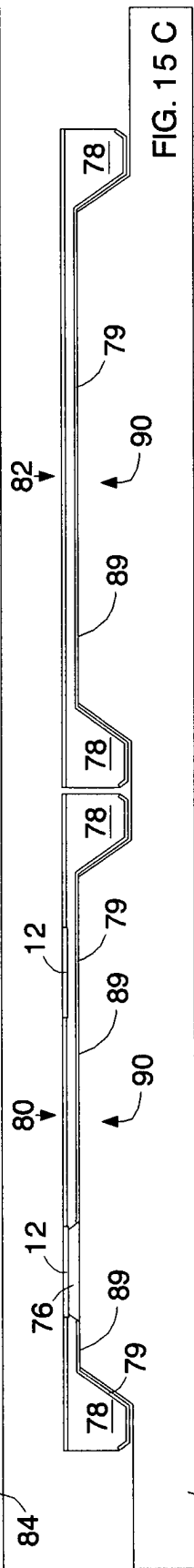
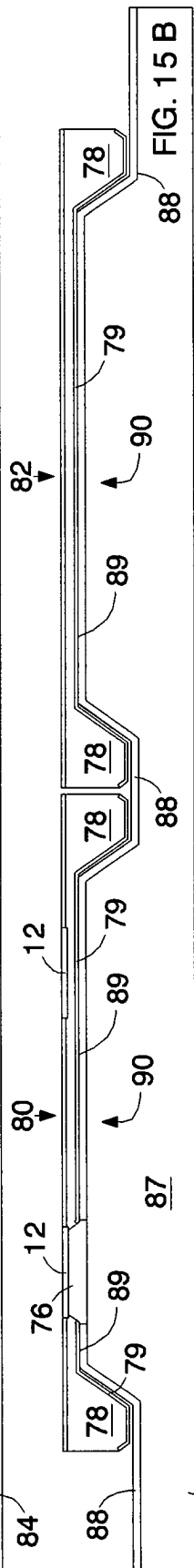
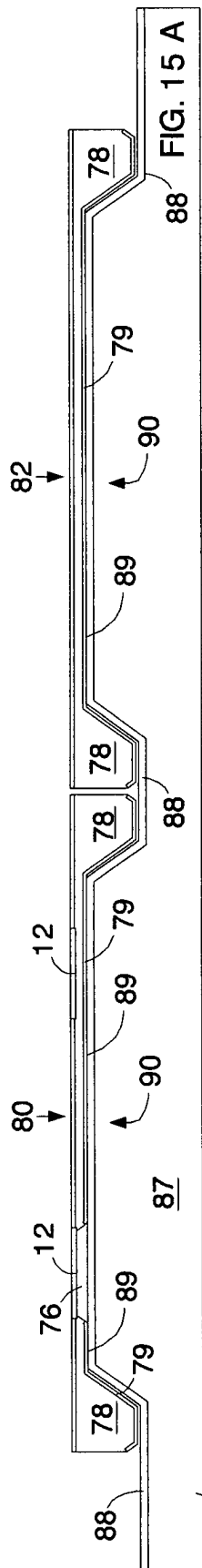


FIG. 14



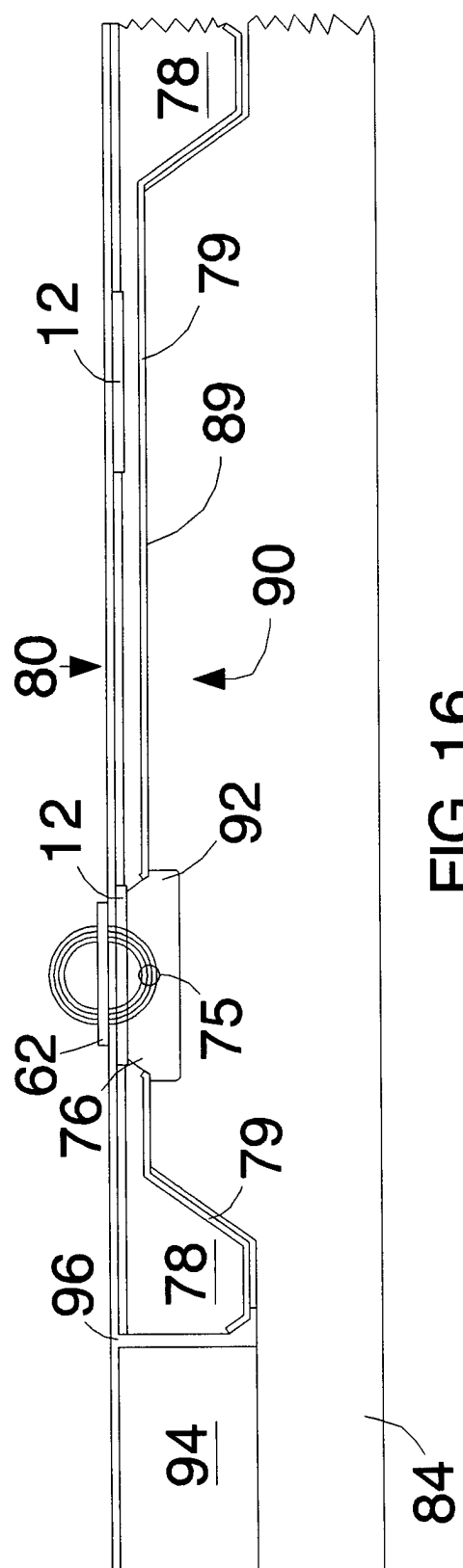


FIG. 16

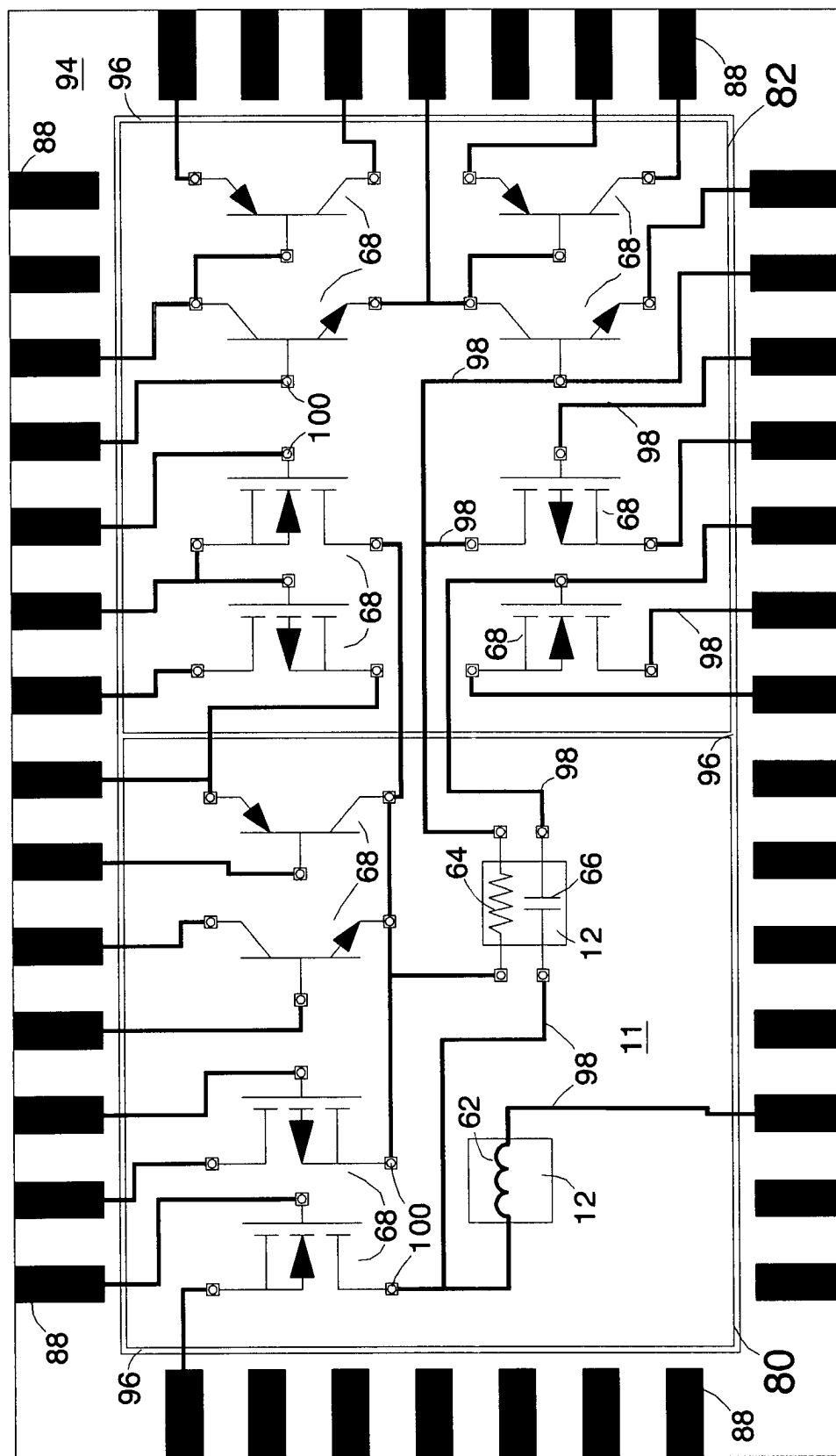


FIG. 17